IN THE CLAIMS:

Please amend the claims as follows.

1. (Original) An instruction segment comprising a plurality of instructions stored in sequential positions of a cache line in reverse program order.

2. (Original) The instruction segment of claim 1, wherein the instruction segment is an extended block.

3. (Original) The instruction segment of claim 1, wherein the instruction segment is a trace.

4. (Original) The instruction segment of claim 1, wherein the instruction segment is a basic block.

5. (Original) A segment cache for a front-end system in a processor, comprising a plurality of cache entries to store instruction segments in reverse program order.

6. (Currently amended) Apparatus ~~The segment cache of claim 5, further~~ comprising:
an instruction ~~storage~~ cache system,
an instruction segment system, comprising:
a fill unit provided in communication with the instruction cache system,
~~wherein~~ the segment cache of claim 5 ~~is~~ included therein, ~~within the instruction segment system,~~ and
a selector coupled to an ~~the~~ output of the instruction cache system and to an output of the segment cache.

7. (Original) The front-end system of claim 6, wherein the instruction segment system further comprises a segment predictor provided in communication with the segment cache.

8. (Original) A method for storing instruction segments in a processor, comprising:
building an instruction segment based on program flow, and
storing the instruction segment in a cache in reverse program order.

9. (Original) The method of claim 8, further comprising:

building a second instruction segment based on program flow, and

if the first and second instruction segments overlap, extending the first instruction segment to include non-overlapping instructions from the second instruction segment.

10. (Original) The method of claim 9, wherein the extending comprises storing the non-overlapping instructions in the cache in reverse program order in successive cache positions adjacent to the instructions from the first instruction segment.

11. (Original) The method of claim 8, wherein the instruction segment is an extended block.

12. (Original) The method of claim 8, wherein the instruction segment is a trace.

13. (Original) The method of claim 8, wherein the instruction segment is a basic block.

14. (Original) A processing engine, comprising:

a front end stage to build and store instruction segments in reverse program order, and

an execution unit in communication with the front end stage.

15. (Currently amended) The processing engine of claim 14, wherein the front-end stage comprises:

an instruction cache ~~storage~~ system,

an instruction segment system, comprising:

a fill unit provided in communication with the instruction cache system,

a segment cache, and

a selector coupled to an ~~the~~ output of the instruction cache system and to an output of the segment cache.

16. (Currently amended) The method of claim 15, wherein the instruction segments are ~~is an~~ extended blocks.

17. (Currently amended) The method of claim 15, wherein the instruction segments are ~~is a~~ traces.

18. (Currently amended) The method of claim 15, wherein the instruction segments ~~is a~~ are basic blocks.

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19. (Currently amended) The processing engine of claim 15, wherein the ~~extended~~ instruction segment cache system further comprises a segment predictor provided in communication with the segment cache.